IN THE CLAIMS:

Please cancel claims 8-18 without prejudice or disclaimer, amend claims 1-7, and add a new claim 19 as follows:

1. (Currently Amended) A semiconductor memory device [[cell]] comprising:

a plurality of first wirings, each of which is located along a first direction with a first wiring pitch;

a plurality of chalcogenide material layers, each of which is located along said first direction;

a plurality of second wirings, each of which is connected with a corresponding one of said chalcogenide material layers, and is located over said corresponding one of said chalcogenide material layers and along said first direction; and

a plurality of vertical transistors, each of which is formed over said corresponding one of said first wirings and under a corresponding one of said second wirings and [[, which]] is comprised of a source region, a drain region, a channel region sandwiched between said source region and said drain region, a gate insulating film formed on all sides of [[along]] said channel region and a gate electrode formed on said gate insulating film and surrounding said all sides of said channel region, ~~wherein said gate electrode is separated from each other along said first direction, but connected from each other along~~

~~a second direction intersecting at right angle with said first direction;~~

~~a plurality of chalcogenide material formed over said drain region; and~~

~~a plurality of second wiring connected with said chalcogenide material, and located over said chalcogenide material along said first direction with a second wiring pitch,~~

wherein said drain region is electrically connected with said corresponding one of said second wirings through corresponding one of said chalcogenide material layers,

wherein said source region is electrically connected with said corresponding one of said first wirings,

wherein gate electrodes of two adjacent ones of said vertical transistors in a second direction, which intersects perpendicularly with said first direction, are connected with each other, and

wherein gate electrodes of two adjacent ones of said vertical transistors in said first direction are separated from each other.

2. (Currently amended) A semiconductor memory device [[cell]] according to claim 1, further comprising:

~~wherein~~ a plurality of plugs,

wherein said source region is electrically connected with said corresponding one of said first wirings through a corresponding one of said plugs ~~is formed between said first wiring and said source region~~.

3. (Currently amended) A semiconductor memory device [[cell]] according to claim 1, wherein a barrier film is formed between said chalcogenide material and said drain region.

4. (Currently amended) A semiconductor memory device [[cell]] according to claim 3, wherein said barrier film is one of TiAlN or oxide of TiAlN or WTi, or laminated films of either of TiAlN or oxide of TiAlN or WTi, or ITO.

5. (Currently amended) A semiconductor memory device [[cell]] according to claim 1, wherein an area of said chalcogenide material connected to said drain region is smaller than an area of said drain region.

6. (Currently amended) A semiconductor memory device [[cell]] according to claim 1, wherein a chalcogenide material includes at least antimony and tellurium.

7. (Currently amended) A semiconductor memory device [[cell]] according to claim 1, further comprising:

a plurality of word lines, each of which extends along said second direction with a word line pitch and is comprised of said gate electrodes which are connected with each other in said second direction,

wherein said first wiring pitch is smaller than said word line ~~second wiring~~ pitch.

8-18. (Cancelled)

19. (New) A semiconductor memory device according to claim 7, wherein said gate electrode is formed by a side wall surrounding said source region, said channel region and said drain region.